Buffering strategies for optical packet switches

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Abstract

Strategies for buffering fixed-length optical packets are discussed, including the use of wavelength to assist in contention resolution, and the implementation of buffers of varying depths using differing technologies, both with and without deflection routing.

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Introduction

Optical packet switching has been researched for a number of years, in anticipation of solving the EMI and pinout problems that will be encountered in future large electronic packet switch cores. In order to overcome these problems, optical packet switches have an entirely optical data path, although they are electronically controlled. The electronic controller operates at a speed equal to the number of packets per second, rather than the line bitrate. A key issue is the manner in which packet contention for each output is resolved [1], since packets arrive at different switch inputs asynchronously. To surmount the problem of contention, several buffering strategies have emerged for fixed-length packets:

- *Deflection routing* – here there are no buffers, and packets are deflected to the wrong output in the case of contention [2]. They are left to reach the destination node by an alternative route.
- *Use wavelength to reduce the amount of buffering* [3,4] – this takes place in the Wavelength Switched Packet Network. Statistical multiplexing between wavelengths reduces the buffering requirement.
- *Use small packet switching modules with a moderate amount of buffering and deflection routing* [5,6], as in Photonic Integrated Gigabit Switches.
- *Imitate electronics by implementing deep buffers*, as in the Switch with Large Optical Buffers [7].

This paper will consider the latter three strategies in turn, discussing an approach to implementing each. Throughout, buffering is carried out with optical delay-lines, due to the non-availability of optical random access memory.

Wavelength Switched Packet Network (WASPNET)

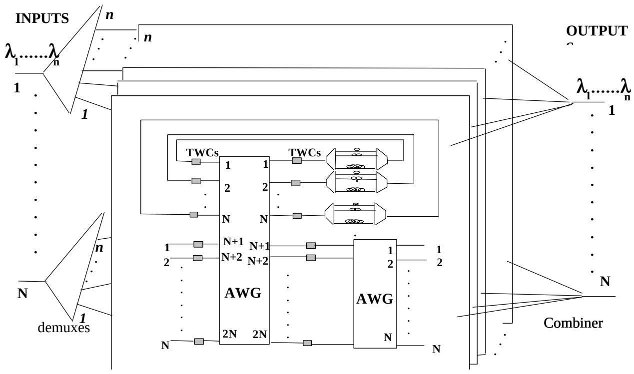

Figure 1: The WASPNET switch. Each plane handles inputs from a different wavelength, although each plane may output packets on more than one wavelength.

In the EPSRC-funded WASPNET project, WDM is used to transport packets between nodes, and also to facilitate contention resolution; each packet is dynamically converted to a suitable wavelength in each link. This decision is influenced by the availability of free timeslots on each wavelength when forwarding to the next node. Suppose there are 16 wavelengths within a particular fiber link carrying a number of optical paths. Every packet directed along the fiber can be transmitted on any of the 16 wavelengths; contention between any two packets being transmitted simultaneously is resolved in the first instance by transmitting them each on a different wavelength. If this fails due to all wavelengths being occupied, buffering is employed to delay some of the packets until a free timeslot is available. Employing wavelength to resolve contention in this way reduces the required buffer capacity, for example at a packet loss rate of 10^{-5} and a load of 0.9, this scheme offers a buffer size reduction of over three times compared to other methods. Analytical studies indicate that a packet loss as low as 10^{-12} may be obtained at a load of 0.7 per wavelength and a buffer depth of only 9 per wavelength [4].

A switch architecture has been designed to implement this contention resolution strategy (Figure 1), with a novel aspect being the use throughout of feedback fiber delay lines with arrayed waveguide gratings – AWGs. Feedback delay lines allow the implementation of multiple packet priorities, while wavelength routers exhibit low loss and low crosstalk, offering superior systems performance. The architecture can be said to implement a shared buffer, since each delay line is not associated with a particular output, but implements buffering for all outputs. Further details of the architecture may be found in Reference 4.

Testbed construction has thus far concentrated on the construction of other architectures using the same components i.e. wavelength converters, AWGs and delay-lines [8]. Further work will involve realizing proof-of-principle demonstrations of the WASPNET architecture detailed above.

Photonic Integrated Gigabit Switches (PIGS)

This switch architecture (Figure 2 [6]) implements much the same function as an output-buffered 2×2 optical packet switch. It is designed to implement a moderate buffer depth, and to operate in conjunction with a limited amount of deflection routing. The delay-lines between switch devices increase in powers of two, starting at one timeslot, and the size of the shared buffer is equal to the sum of all the delay-line lengths i.e. $2^{k-1} - 1$, where k is the number of switches. As part of the EPSRC-funded PIGS program, the buffered switch is being fabricated on a silicon substrate with silica delay-lines, which may be up to 4m in length [9].

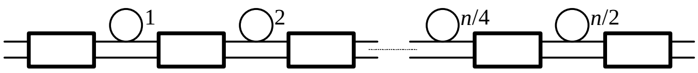

Figure 2: 2x2 switch architecture; the buffer depth rises exponentially with the number of switches.

The 2×2 switch devices have been fabricated from quantum well epitaxial structures based on InGaAs/InGaAsP/InP laser structures and operate in the communications wavelength range around 1.55µm. The layout of the switch is shown in Figure 3. The switches consist of 2×2 multi-mode interference (MMI) couplers integrated with amplifiers and modulators. The MMI couplers are designed to split light input to either of its two input ports equally between its two output ports, while the amplifiers compensate for coupling and interface losses, as well as losses in the passive sections of the III-V semiconductor chip. Electroabsorption modulators are used to modulate the signals, since they operate faster than amplifiers. A further advantage of this arrangement is that the amplifiers are run cw, so imposing a constant thermal load on the chip.

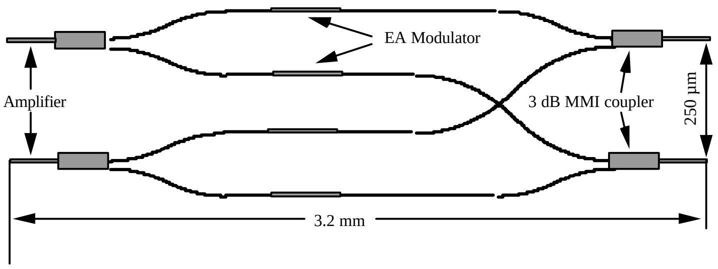

Figure 3: Schematic of the 2x2 crosspoint switch.

The fabrication of the monolithically integrated 2×2 switches requires the realization of three different bandgaps on a single substrate. The optimum bandgap for the modulators is larger than that required for the amplifiers and smaller than that required for the low loss waveguides. In order to engineer these three bandgaps after growth, quantum well intermixing (QWI) has been carried out to tune the bandgap in selected areas of the device chips, using a sputtered SiO_2 technique [10]. Finally, the MMI couplers and waveguides were defined using a single photolithographic step and a Ti/Si_3N_4 mask. The devices were reactively ion etched in a $CH_4:H_2:O_2$ plasma using a process described in Reference 11.

Switch with Large Optical Buffers (SLOB)

A final approach involves implementing deep buffers, in order to attain the buffer depth required for bursty traffic. This is implemented by the Switch with Large Optical Buffers (SLOB [7] – Figure 5) which cascades many small switch elements, forming a larger switch with a greater buffer depth. A modified Alcatel OASIS switch [12] is chosen as the basic switch element, although other switches could be used. SLOB is electronically controlled but has an optical packet data path, with *m* inputs and outputs. The delay line lengths increase exponentially from left to right along the structure, and each buffer has a depth of $m^k - 1$ packets, where *k* is the number of stages in the architecture, hence the number of stages increases with the logarithm of buffer depth. It emulates an output-buffered switch, thus exhibiting optimal delay/throughput performance. Experiments have shown that 40 similar stages may be cascaded with the aid of optical regeneration [13], further justifying this concept.

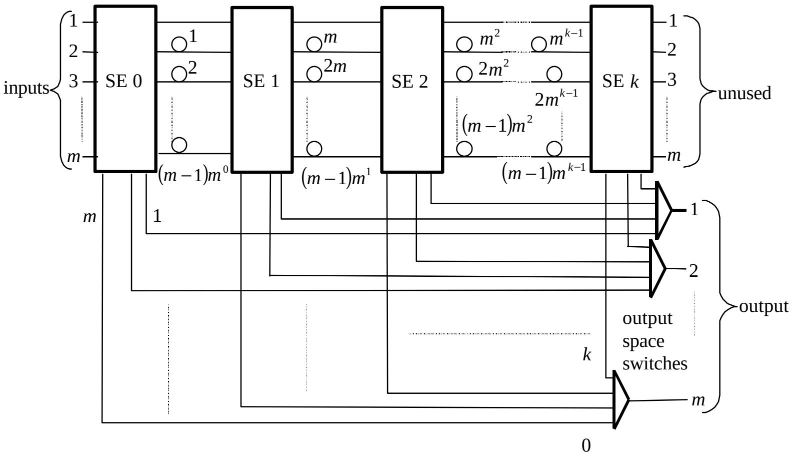

Figure 4: SLOB architecture; each stage is a modified OASIS switch (SE or switch element).

Conclusions

The three major buffering strategies for optical packet switching have been identified, and examples of work in each have been discussed. These were based on using statistical multiplexing among many wavelengths to relax buffering requirements, using deflection routing in conjunction with some buffering, and implementing deep buffers. It is certainly too early to say which technique will predominate, however it is likely that WDM will be used in conjunction with optical packet switching in order to enhance the link capacity.

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