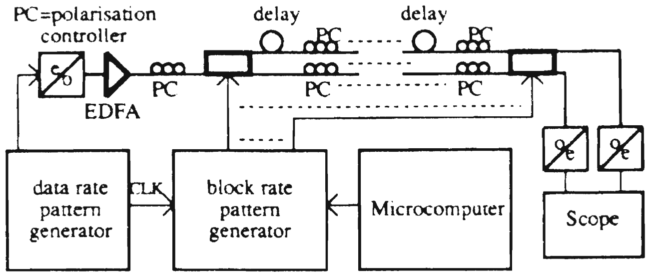
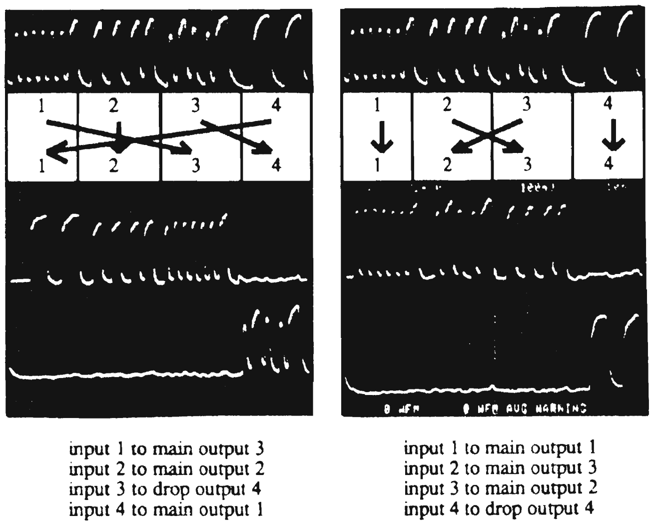


TuO2 Fig. 1. Experimental time slot interchanger test bed configured for systems with one input.



TuO2 Fig. 2. Experimental operation of a 4-time slot TSI for 720-Mbit/s data with 45-Mbit/s blocks. Time slots are numbered from 1 to 4, and the arrows illustrate the mapping of inputs onto outputs.

TuO2 5:00 pm

Experimental test bed for optical time-domain switching fabrics

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Optical time-division multiplexing will be an important technique in future optical networks for transmission of high-speed continuous-bit-rate services and transport of ATM. Optical switching has the advantage over electronics of permitting transparency to bit rate, coding format, and wavelength.

Here we introduce experimental demonstration of a new class of optical time slot interchangers consisting of 2 × 2 switches and delay lines. They are a subset of a family of more complex switch architectures[1] that have been proposed theoretically, and they overcome many of the limitations of previous work (e.g., Ref. 2) by using feedforward delays. Network control is accomplished by adapting standard control algorithms. Our test bed will be used in the future characterization of these fabrics (Fig. 1).

The implementation described here is of an optical time slot interchanger offering a drop function. It consists of three lithium niobate 2 × 2 directional-coupler switches (loss 6–7 dB, extinction 15 dB) and two delay lines, and it switches four channels of 720-Mbit/s data. The architectures are used with block multiplexing for which the switches change state only between blocks; the switching rate (45 Mbit/s) is lower than the optical bitrate. This permits 16 bits per time slot—14 bits data plus 2 bits guard band—to cater to the rise time of the drivers.

An erbium-doped-fiber amplifier was used to overcome losses of approximately 20 dB within the fabric. The last switch was used as a drop output with a block either sent to the main upper output or dropped to the lower output. A microcomputer calculated the switch-control signals required for implementing the mapping of input time slots to output time slots. Figure 2 shows the detected output pulse trains for two switch mappings.

Bit-error-ratio (BER) measurements were made on the dropped channel (Fig. 3) by varying the incident power onto a standard 2.5-Gbit/s receiver with postdetection equalization. Two back-to-back measurements were made (curves 2 and 4) to reference the switch penalties. With four blocks the 10^{-9} sensitivity was −29.6 dBm, and with one block it was −34.8 dBm (the difference was 5.2 dB, not 6 dB, because the data extinction ratio was the same in both cases). With the switch fabric the best-case cross-talk situation gave an improvement in sensitivity of 0.7 dB, where the amplified spontaneous emission (ASE) produced by the EDFA was replaced by the cross talk from the empty time slots. With worst-case cross talk a small penalty was observed (0.3 dB) because of cross talk from full channels.

An experimental demonstration of a member of a new class of time slot interchangers has been performed. A full BER characterization indicated that the fabric exhibits acceptable performance, with no evidence of an error floor The test bed will be used in the future to fully investigate more complex configurations, ATM switching, and other technologies.

1. D. K. Hunter *et al.*, in *Proc. SPIE Multigigabit Fiber Systems*, OE Fibers '92 (Society of Photo-Optical Instrumentation Engineers, Bellingham, WA, 1992)
2. R. A. Thompson, IEEE J. Sel. Areas Commun. **6**, 1096 (1988).

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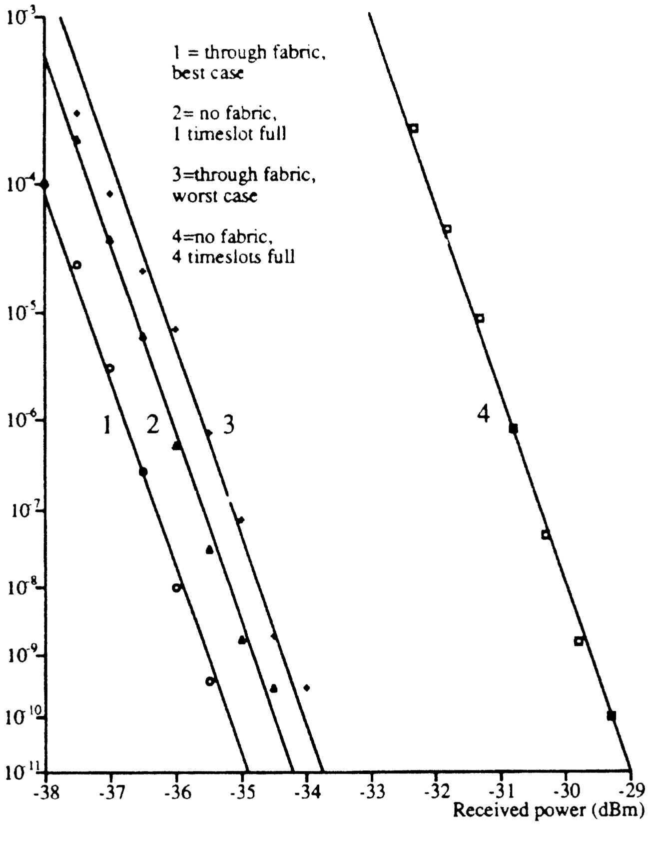

TuO2 Fig. 3. Bit-error-ratio (BER) measurements for the experimental implementation.