Packet Loss and Delay Performance of Feedback and Feed-Forward Arrayed-Waveguide Gratings-Based Optical Packet Switches With WDM Inputs–Outputs

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***Abstract*—This paper analyzes the packet loss and delay performance of an arrayed-waveguide-grating-based (AWG) optical packet switch developed within the EPSRC-funded project WASPNET (wavelength switched packet network). Two node designs are proposed based on feedback and feed-forward strategies, using sharing among multiple wavelengths to assist in contention resolution. The feedback configuration allows packet priority routing at the expense of using a larger AWG. An analytical framework has been established to compute the packet loss probability and delay under Bernoulli traffic, justified by simulation. A packet loss probability of less than 10^{-9} was obtained with a buffer depth per wavelength of 10 for a switch size of 16 inputs–outputs, four wavelengths per input at a uniform Bernoulli traffic load of 0.8 per wavelength. The mean delay is less than 0.5 timeslots at the same buffer depth per wavelength.**

***Index Terms*—Modeling, optical communications, optical packet switching, photonic switching systems, switch architecture, wavelength-division multiplexing.**

I. Introduction

DUE TO the electronic bottleneck, the full potential of optical transmission cannot be harnessed in switched systems employing electronic nodes in the transmission path. To overcome this problem, WASPNET [1], a multi-institution project funded by the United Kingdom's Engineering and Physical Sciences Research Council (EPSRC) and supported by industry, is proposed as one solution to the continually growing demand for telecommunication transport capacity. It is a packet-based transport network that can initially support conventional optical paths for interfacing to SDH/SONET and can then inherently evolve toward transporting and switching optical packets. Optical packet switching has the potential for high speed, data rate transparency, data format transparency, fine granularity, and flexibility [2].

In packet-switched networks, information is encapsulated in packets consisting of a header and a payload. The header contains (among other things) information pertaining to the packet destination, while the payload carries the information itself. Fast packet switching that uses fixed-length packets (cells) such as the asynchronous transfer mode (ATM) [3] has been deployed to support a wide range of communication services of different statistical natures, supporting bit rates ranging from several Kb/s to hundreds of Mb/s. In a conventional time-division multiplexed system, the channel that each timeslot belongs to is dictated by its position within a frame; in ATM, each packet (or "cell") has its channel identified by the virtual channel indicator (VCI) in the header.

A packet switch has three principal functions: *switching*, *buffering*, and, optionally, *header translation*. *Switching* ensures that each packet emerges at the correct output, depending on the information contained in the packet header. Although packets arriving on the inputs have to be synchronized, there is no coordination between packet streams arriving on different inputs. Hence, one or more packets may arrive during the same timeslot on different inputs wishing to go to the same output. For this reason, *buffering* is required. An important factor when designing packet switches of any kind is contention resolution, since multiple packets may arrive asynchronously at the same time to go to the same output.

The implementation of an effective buffering strategy directly in the optical domain is crucial to the design of optical packet switches. Since optical random-access memory (RAM) is not as yet a practical option, delay lines (usually made from optical fiber) must be used to store and buffer optical packets. Here, wavelength also assists in contention resolution, where contending packets may be transmitted on different wavelengths, reducing the optical delay-line buffering requirements.

In addition to using wavelength, the proposed WASPNET node buffers packets to resolve contention, using optical delay lines, and transmits them when the relevant output link is available. Also, when priority routing is employed, the buffered packet's priority is increased after each time unit. In this paper, priority routing is assumed throughout the design process.

Header translation represents a central process in the ATM transmission systems strategy. At every switch in a route, the

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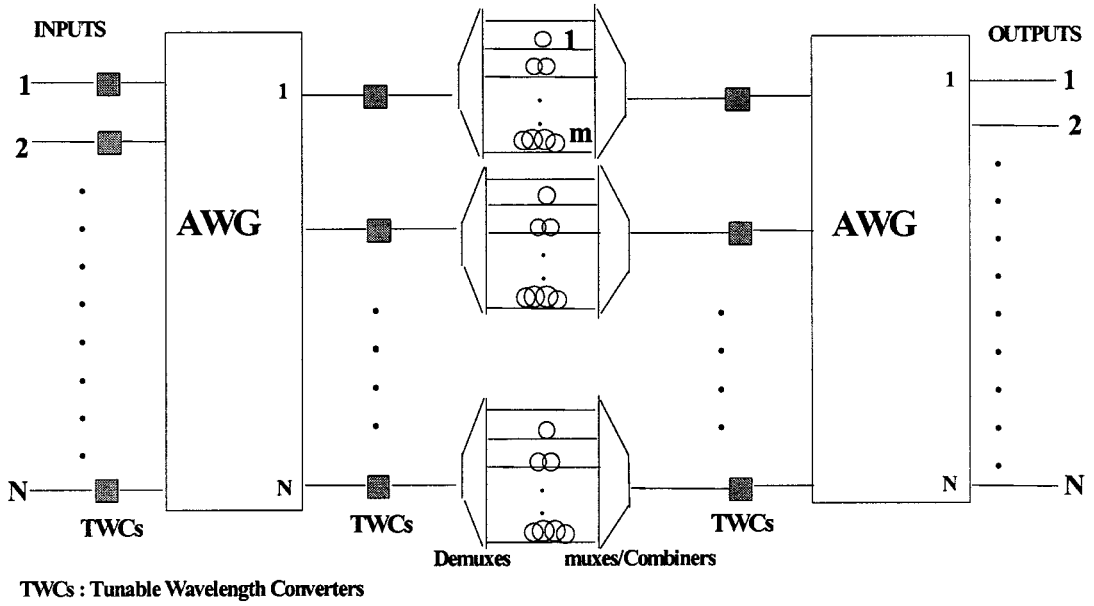

Fig. 1. A feed-forward AWG-based optical packet switch.

VCI value is looked up in a table; from the table, the new value of the VCI and the output port that the packet must go to is determined. The new VCI is substituted for the old one in the packet header. While these schemes offer great functionality and flexibility, they are not used in every optical packet-switching system since header translation directly in the optical domain is in the early stages of development. The header is usually at a lower bit rate than the payload to facilitate the decoding and interpretation of header information in the electronic domain. An alternative header organization is used in the Internet, and much work [4], [5] has focused on the development of data structures and algorithms for minimizing the lookup time given routing table and memory space constraints.

Throughout, it is assumed that time is divided into equal timeslots, each containing one optical packet. The development of optical packet switching thus far has largely concentrated on utilizing packets of fixed duration, simplifying the design and operation of the network and switching nodes. The transport of larger entities (e.g., IP datagrams) is achieved by segmenting them into smaller, equal packets at the interfaces of the electronic and optical layers. It is assumed that packets entering the switch are aligned with respect to their boundaries, so that each packet is aligned with its timeslot. Such synchronization is generally a requirement for correct switch operation; approaches to achieving packet synchronization at the inputs to the switches constitute a topic in their own right [6] and will not be discussed further.

There has been much work on the design of optical packet switches [7]–[18], the common limitation being optical splitting loss that is compensated by optical amplifiers, which in turn can degrade performance because of the induced amplifier noise [19]. Some existing switches [7]–[18] were initially considered as candidates for the WASPNET node. Because wavelength is used to assist in contention resolution, only a small physical buffer depth is required in the WASPNET node, so SLOB [8], which provides a large buffer depth, is not suitable. Wave Mux [9] has a complex routing procedure and introduces a significant delay for large networks. In addition, since feedback delay lines are preferred, this switch using feed-forward delay lines is not considered.

Some architectural concepts in the switch based on WDM [12] can be modified and incorporated into the WASPNET node; for example, the demultiplexing of inputs in front of the node and the shared buffer concept. The recirculating loop concept [13], [14] is also used in the WASPNET node. Some concepts used in the staggering switch [15] are incorporated into the proposed switch, i.e., the buffering stage and the switching stage.

A simple architecture and routing procedure are the main features and advantages of the ALCATEL switch [16]–[18]. Although feed-forward delay lines are used, it can select appropriate channels using semiconductor optical amplifier (SOA) gates. This switch fulfills many of the WASPNET node requirements and has also been the subject of substantial development.

Here the design strategy centers on the use of arrayed waveguide grating devices (AWGs) with low crosstalk levels (as low as -30 dB [20]) to reduce the optical splitting in both feed-forward and feedback configurations.

In this paper, two proposed node configurations are discussed in Section II. Their scheduling operations are presented in Section III, and the analysis of their packet loss performance is illustrated in Section IV. The analytical results and their justification by simulation are described in Section V.

Throughout, there are N inputs and outputs on the node, each carrying n wavelength channels.

II. Proposed Switch Architecture and Operation

In the feed-forward architecture depicted in Fig. 1, the input packets are converted to the wavelength that facilitates switching to the correct output of the first AWG. Each AWG output is connected via a tunable wavelength converter to a number of fiber delay lines, which lie in parallel between a

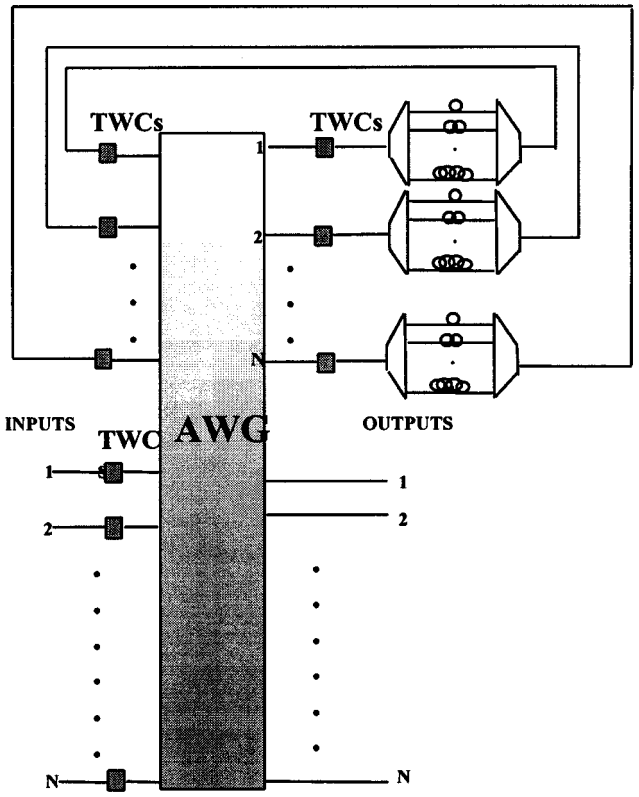

Fig. 2. A feedback architecture with a total of mN delay lines.

demultiplexer and a multiplexer. Each fiber entering the second AWG carries no more than one wavelength channel, because the tunable wavelength converter there only converts a single wavelength at one time. Therefore, the controller must ensure that no more than one packet leaves a multiplexer at once.

If no first AWG output is available, the packet must then be stored in a longer delay line than otherwise, in order to find a free output. This kind of contention is called exit time contention for the reminder of this paper. Scheduling will be addressed in detail in the next section. The second AWG routes the packets to the outputs according to the wavelengths produced by the third column of wavelength converters.

The feedback architecture shown in Fig. 2 requires only one $2N \times 2N$ AWG. It uses shared feedback delay lines to buffer the contended packets and also allows high-priority packets to preempt low-priority packets, a feature not present in the feed-forward architecture. First, input packets are converted to the correct wavelengths; the contended packets are routed to the recirculating loops for buffering while the straight-through packets are routed to switch outputs. Only one packet may exit from each multiplexer in the loop at a time. The control is much the same as before; no more than one packet may exit from each combination of fiber delay lines, a demultiplexer and a multiplexer; otherwise it will be routed to other alternative AWG outputs or, if necessary, to longer delay lines. This architecture allows implementation of priority routing. If a higher priority input packet is destined for the same output as the buffered packet, the buffered packet will be switched to the feedback delay lines again and the input packet having higher priority is switched straight through. The number of fiber delay lines necessary for a required cell loss probability is dependent on traffic.

A. WDM AWG-Based Optical Packet Switch

The above architecture has single-wavelength inputs and outputs but can be modified to handle WDM inputs–outputs (Fig. 3). All the input wavelength channels are demultiplexed to n (number of wavelength channels per input) parallel planes, each containing the optical packet switch of Fig. 2, plus an additional stage of wavelength converters, and a many-to-one space switch. A combiner instead of a multiplexer is required to merge the wavelength channels from all planes, allowing dynamic wavelength allocation at each plane.

If the space switch were omitted, this would limit operation to only one wavelength per plane output port because tunable wavelength converters can only handle one incoming wavelength at a time. After undergoing the necessary delay, the AWG routes the packets to the space switch via a wavelength converter. Hence each packet is switched to the correct output port at the correct transmission wavelength via the final stage of wavelength conversion and the space switch. The many-to-one space switch permits multiple packets to leave the same output on the same plane simultaneously, but on different wavelengths, permitting sharing of capacity between wavelengths to take place.

The design of the proposed node has been evaluated and compared with other existing optical packet switches.

1) The feedback configuration enables the implementation of priority routing where high-priority packets preempt low priority ones.
2) In the switch using a single loop for buffering [13], [14], unlike the proposed node, the number of packets in the loop scheduled in previous timeslots greatly limits the number of packets that can be stored in the future timeslots because they overlap in space. In addition, the buffer depth depends on the maximum achievable number of the circulations, which is limited by the accumulated ASE noise.
3) In the ALCATEL switch [16]–[18], the buffer depth is determined by the splitting loss that can be significant for a large buffer depth. The buffer depth in the proposed node depends on the size of the multiplexer/demultiplexer or an AWG.
4) The use of AWG devices in the proposed architectures has been shown to require fewer components (especially SOA gates) than the broadcast-and-select switch. For large switch sizes, the splitting loss will limit the broadcast-and-select switch performance, whereas the proposed architecture can be easily scaled up to 32 inputs. The number of SOA gates used in the ALCATEL switch increases quadratically with the number of inputs–outputs. However, the number of tunable wavelength converters in the proposed architecture is equal to roughly only three times the number of inputs–outputs.
5) The switch proposed in [21] is also a two-stage architecture but does not have WDM inputs–outputs. The proposed switch in this paper is modified to handle WDM

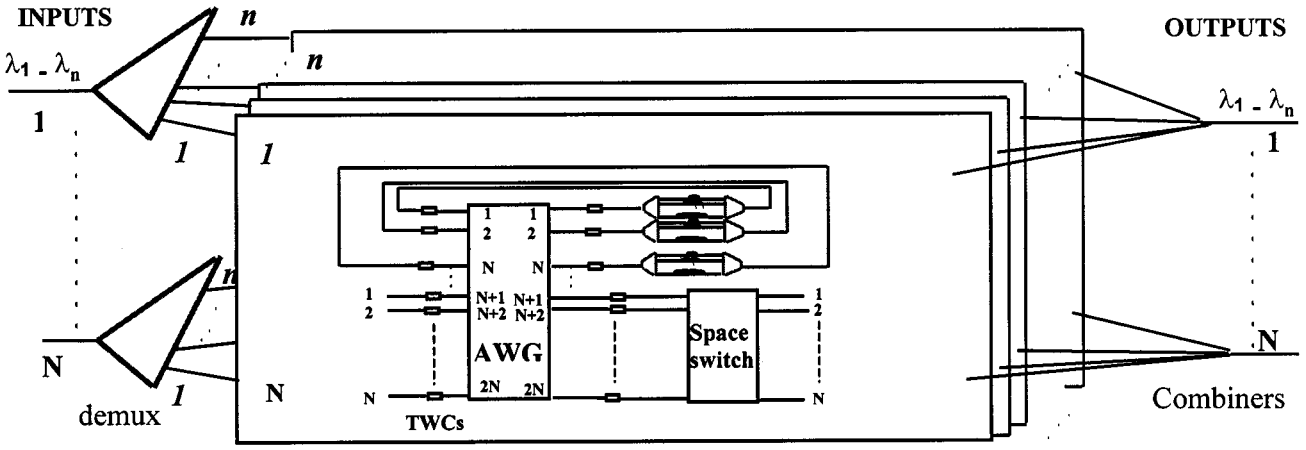

Fig. 3. WDM version of the packet switch.

inputs–outputs and uses only one AWG per plane to perform the same node functions.

6) A similar node architecture with feed-forward delay lines has been proposed in [22]. It does not facilitate priority routing.

III. Scheduling

A. FIFO or Non-FIFO?

Without first-in–first-out (FIFO) operation, it is possible for a packet to overtake another packet that entered the switch later, causing packet misordering and requiring the implementation of packet resequencing. With an FIFO scheduling algorithm, the sequence of packets in the same optical path [23] is preserved. In the multiplane configuration, a packet will be routed to an output port if there is:

1) no output port contention;
2) an available wavelength at the output of a plane;
3) no exit time contention;
4) the packet sequence order is kept.

Unlike FIFO, a non-FIFO scheduling algorithm does not preserve the sequence order of packets belonging to an optical path; i.e., in the multiplane configuration, a packet will be routed out even if only the first three conditions above are met.

Here, these two scenarios were simulated in terms of their packet loss and delay performance. Comparison of the results in Figs. 4 and 5 shows that keeping the packet sequence order (FIFO) has an insignificant effect on the packet loss and delay performance. This behavior might be attributed to the high traffic load adopted in the simulation, making it unlikely that a wavelength in any timeslot is available. There are fewer opportunities for a packet to overtake another packet that entered the switch later. However, Figs. 6 and 7 show that even under a traffic load of 0.5, the influence of the control algorithm is insignificant.

The scheduling operation described here is therefore based on FIFO scheduling since it does not increase packet loss or delay but preserves the packet sequence.

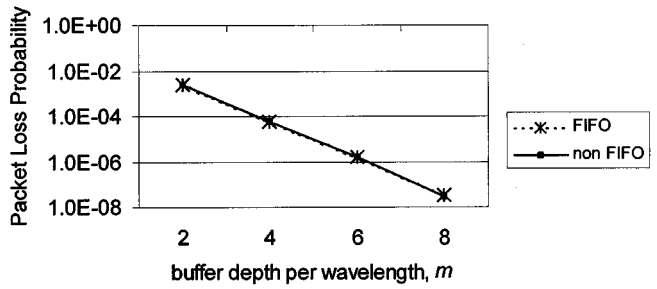

Fig. 4. Packet loss performance comparison between FIFO and non-FIFO control algorithm for $N = 16$, $n = 4$, and uniform traffic of 0.8 per wavelength (simulation results).

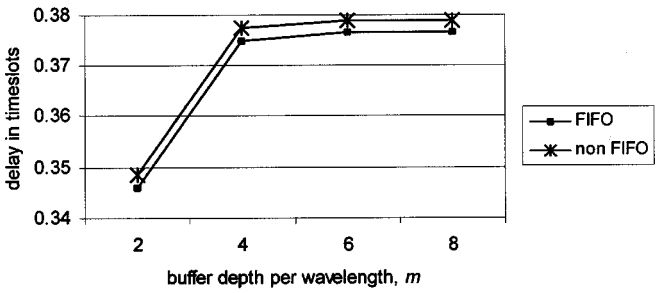

Fig. 5. Delay performance comparison between FIFO and non-FIFO control algorithm for $N = 16$, $n = 4$, and uniform traffic of 0.8 per wavelength (simulation results).

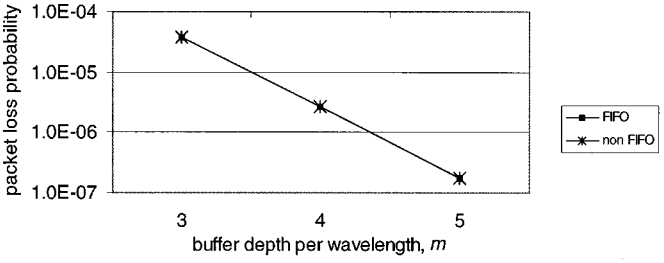

Fig. 6. Packet loss performance comparison between FIFO and non-FIFO control algorithm for $N = 16$, $n = 2$, and uniform traffic of 0.5 per wavelength (simulation results).

B. Scheduling

This section concentrates on packet scheduling in the presence of exit time contention. The analysis in this paper refers to

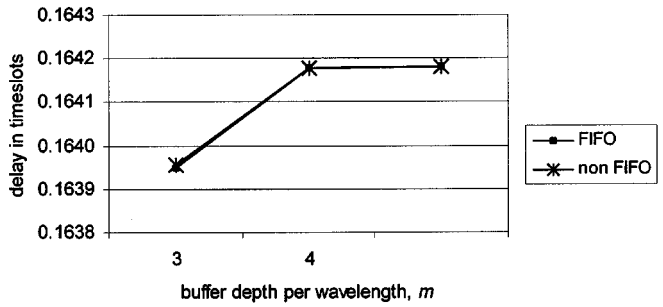

Fig. 7. Delay performance comparison between FIFO and non-FIFO control algorithm for $N = 16$, $n = 2$, and uniform traffic of 0.5 per wavelength (simulation results).

Fig. 1, although this also applies to Fig. 2 with one circulation. At most one packet in any timeslot may be routed to each tunable wavelength converter feeding into the second AWG. For example, at timeslot i, if a packet's predetermined delay is d timeslots, a delay line providing that delay and associated with a third-stage tunable wavelength converter (WC) is only available if no other packets are also scheduled to transmit during timeslot $i + d$ to the same tunable WC. In other words, only one packet is allowed to exit from each set of delay lines in a timeslot. For a particular packet, if the above condition cannot be fulfilled for all sets of delay lines, the packet must be stored in a longer delay line or it will be lost.

In addition, at each timeslot, up to N packets may wish to go to an output of a plane. More than one packet can be switched to one plane output (provided only up to n wavelengths are routed out to each switch output from all planes) at each timeslot if one or more other outputs do not have a packet destined for them. For example, at timeslot j, suppose there are two packets destined for output i, which has no packet in its queue. Both can therefore be routed to output i at once if only $N-2$ or fewer packets are scheduled for switching to the $N-1$ other outputs at timeslot j. First, the controller determines the appropriate delays for all input packets so that only N packets are routed to the switch outputs in each timeslot in the following order, subject to the FIFO discipline.

1) Ensure the packet sequence is kept.
2) Only n packets can be routed to each switch output from all the n planes, i.e., no output port contention.
3) Only a maximum total of N packets are routed from each plane in each timeslot.

The pseudocode in the Appendix addresses the scheduling process during a timeslot in detail.

IV. Packet Loss Probability

A. Analysis Assumptions

The analysis in [23] considers a WDM queue without any internal blocking; the packet loss probability analysis here is extended from this work and considers only fixed-length packets. The architecture in Fig. 1 is used for the analysis since it is an unfolded version of the feedback geometry of Fig. 2 and both yield the same packet loss probability. For simplicity, it is assumed that independent Bernoulli processes govern input packets, and packets on all inputs are uniformly distributed among all switch outputs. In reality, traffic is much more demanding; Internet [24] and voice traffic [24] can be modeled by Pareto and exponentially distributed statistics, respectively. Here, the input packet statistics are modeled as Bernoulli processes because it is the simplest distribution, resulting in a tractable analysis while still yielding an appreciation of switch performance.

To facilitate the analysis further, the queue size of a particular output referred to as the "tagged" output is focused upon. From Fig. 2, N is the number of inputs and outputs, m is the number of fiber delay lines in each set, and n is the number of wavelength channels per input or output. All switch inputs and outputs are multiwavelength, where there may be up to n wavelengths present on each input/output. Therefore, a maximum of nN wavelength channels are switched. The probability of a packet's arriving at one of these nN input wavelength channels is ρ_{in}, and hence for uniform traffic, the probability that there is an input packet destined for a given output is ρ_{in}/N. Consequently, the probability of i packets' wishing to go to the tagged output from all N inputs is given by a Binomial distribution

$$\begin{aligned} a_i &= P[Z = i] \\ &= \binom{nN}{i} \left(\frac{\rho_{\text{in}}}{N}\right)^i \left(1 - \frac{\rho_{\text{in}}}{N}\right)^{nN-i}, \\ & \qquad i = 0, 1, 2, \ldots, nN. \end{aligned} \tag{1}$$

Packet arrivals are assumed to be independent. The steady-state number of packets destined for different outputs will only be independent if N is large. Nevertheless, these independence assumptions are used here even for finite N to simplify the analysis. The total buffer size M is the maximum number of packets that can be stored for the tagged output

$$M = m \times n.$$

In each timeslot, up to n packets may leave the buffer feeding the tagged output. The steady-state probability of i packets scheduled to leave consecutively from the tagged output buffer is defined as q_i, when, if j packets remain in the buffer, $\min(j, n)$ leave on each timeslot. For example, q_5 is the probability of there being five packets in the queue for the tagged output, and if $n = 4$, four of the buffered packets have a one-timeslot delay and another one has a two-timeslot delay. It is assumed throughout that packets are always scheduled to leave on consecutive timeslots. The last packet in the queue experiences a delay of $\lceil i/n \rceil$, where $\lceil y \rceil$ is the smallest integer greater than or equal to y. Fig. 8 illustrates the buffer associated with the tagged output.

B. Derivations of Associated Parameters

1) Probability of No Exit Time Contention: For the sake of mathematical tractability, it is assumed throughout that packets are routed to the tagged output before other outputs in each timeslot, thus yielding a lower bound on the loss probability. The exit time contention for the tagged output is considered here. Since, in each timeslot, it is assumed that packets destined for the tagged output will be routed first, exit time contention originates from packets that are scheduled in previous timeslots. Exit time contention is the only reason that a delay

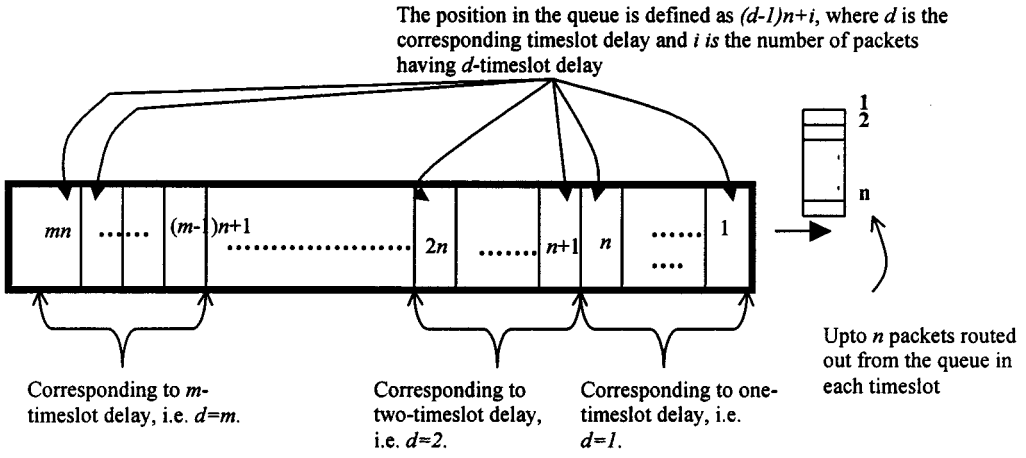

Fig. 8. Illustration of the tagged output's buffer/queue.

line would be unavailable since there are N outputs and N delays of each value, and also, all second-stage tunable wavelength converters will be free since the tagged output is being routed first. $\text{all\_}y\text{\_free}(d, y)$ is the probability that all the y new arriving packets destined to the tagged output do not suffer exit time contention with any of the packets scheduled in previous timeslots for the same third-stage tunable wavelength converters after d-timeslot delays.

Let $\text{pacs\_}d(d, k)$ be the event that represents packets in any d-timeslot delays in the current timeslot where the packets were scheduled in previous timeslots and destined for output port k. This applies to packets scheduled before packets destined to the tagged output are scheduled in the current timeslot. $\text{same\_twc}()$ is the event that any of these packets are routed to the same third-stage wavelength converter as any of the new arriving packets destined to the tagged output after d-timeslot delays. $\text{one\_block}(d)$ is the probability that a particular input packet destined to the tagged output is unable to access a particular third-stage tunable wavelength converter after a d-timeslot delay because it has already been reserved by packets scheduled in previous timeslots, given by

$$\begin{aligned}\text{one\_block}(d) &= \sum_{k=1}^{N} P(\text{pacs\_}d(d, k) \cap \text{same\_twc}()) \\ &= \sum_{k=1}^{N} P(\text{pacs\_}d(d, k)) \cdot P\left(\text{same\_twc}() / \text{pacs\_}d(d, k)\right). \end{aligned} \tag{2}$$

$P(\text{pacs\_}d(d, k))$ is the probability of the output port k's queue being of size $dn+1$ [corresponding to a $(d+1)$-timeslot delay] or more at the beginning of a timeslot. Assuming all the output ports are in equilibrium, $P(\text{pacs\_}d(d, k))$ is then given by

$$p(\text{pacs\_}d(d, k)) = \sum_{w=dn+1}^{mn} q_w \qquad \text{for all } k \tag{3}$$

and $P(\text{same\_twc}()/\text{pacs\_}d(d, k))$ is the probability that a particular packet destined to the tagged output is unable to access a particular third-stage tunable wavelength converter given that there are packets scheduled in previous timeslots competing for the same wavelength converter. This probability is dependent upon on the number of packets scheduled in previous timeslots that are competing for the same stage of tunable wavelength converters, i.e., pacs in the following equation, which in turn is determined by the queue size in (3), w. Therefore, it is given by

$$p\left(\text{same\_twc}() / \text{pacs\_}d(d, k)\right) \approx \frac{\text{pacs}}{Nn}$$

where

$$\begin{aligned} &\text{if } w \le dn + n - 1 \quad [w \text{ is the value from (3)}] \\ &\text{pacs} = w \bmod n \\ &else \\ &\text{pacs} = n. \end{aligned}$$

Nn is the total number of third-stage tunable wavelength converters in all n planes. Therefore, (2) becomes

$$\begin{aligned} &\text{one\_block}(d) \\ &= \sum_{k=1}^{N} P(\text{pacs\_}d(d, k)) \cdot P\left(\text{same\_}wc() / \text{pacs\_}d(d, k)\right) \\ &= P(\text{pacs\_}d(d, 1)) \cdot P\left(\text{same\_}wc() / \text{pacs\_}d(d, 1)\right) \\ &\quad + P(\text{pacs\_}d(d, 2)) \cdot P\left(\text{same\_}wc() / \text{pacs\_}d(d, 2)\right) \\ &\quad + \cdots + P(\text{pacs\_}d(d, N)) \cdot P\left(\text{same\_}wc() / \text{pacs\_}d(d, N)\right) \\ &= \sum_{w=dn+1}^{nN} q_w \cdot \frac{\text{pacs}}{nN} + \sum_{w=dn+1}^{nN} q_w \cdot \frac{\text{pacs}}{nN} \\ &\quad + \cdots + \sum_{w=dn+1}^{nN} q_w \cdot \frac{\text{pacs}}{nN} \quad \text{(for } N \text{ times)} \\ &= N \sum_{w=dn+1}^{nN} q_w \cdot \frac{\text{pacs}}{nN} \\ &= \sum_{w=dn+1}^{nN} q_w \cdot \frac{\text{pacs}}{n}. \end{aligned} \tag{4}$$

For simplicity, Lee's approximation method [25] has been used to estimate the blocking probability due to the third-stage wavelength converters. $\text{all\_}y\text{\_free}(d, y)$ must be known, and it is also necessary to know the probability that all the particular y

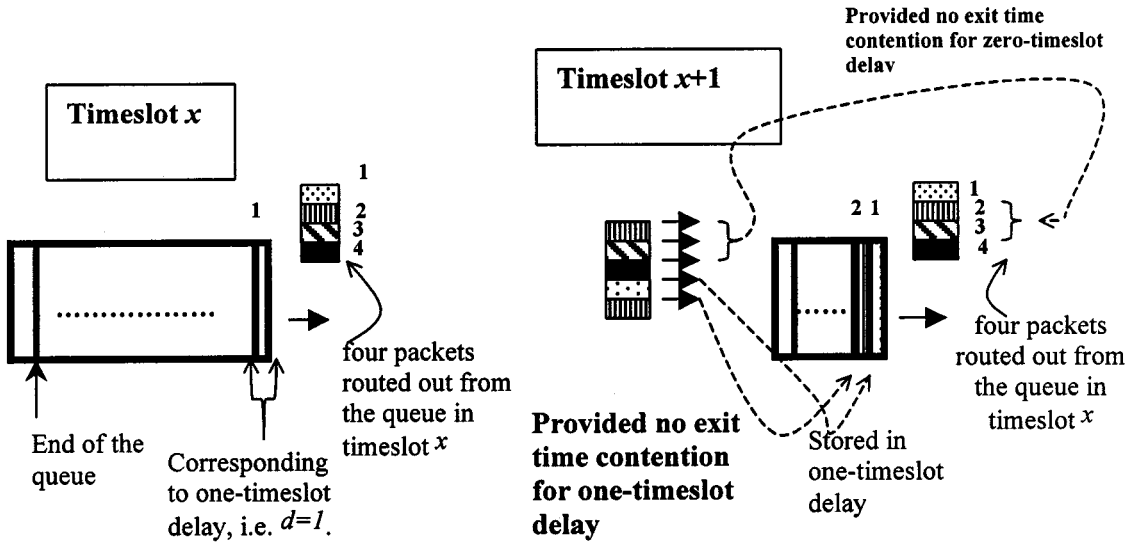

Fig. 9. Example of the transition probability of t_{12}

wavelength converters associated to a d-timeslot delay have not already been allocated

$$\begin{aligned}
&\text{all_}y\text{_free}(d, y)\\
&\quad = P[\text{at least the } y \text{ tunable wavelength converters}\\
&\qquad (d\text{-timeslot}) \text{ are free}]\\
&\quad = \sum_{\text{free}=y}^{nN} (P(\text{one particular tunable wavelength}\\
&\qquad \text{converters is free}))^{\text{free}}\\
&\quad = 1 - \sum_{\text{busy}=nN-y+1}^{nN} (P(\text{one particular tunable}\\
&\qquad \text{wavelength converters is busy}))^{\text{busy}}\\
&\quad = 1 - \sum_{\text{busy}=nN-y+1}^{nN} (\text{one_block}(d))^{\text{busy}} \qquad (5)
\end{aligned}$$

where $\text{one\_block}(d)$ is obtained from (4).

C. Transition Probabilities

The state transition probability t_{ij} for the number of cells in the queue can be obtained using the cell arrival probability a_i. t_{ij} is the transition probability of having j cells in the queue at the end of time slot x given that there were i cells at the end of time slot $x-1$

$$t_{ij} = \begin{cases}
\sum_{l=0}^{n-i} a_l \cdot \text{all_}y\text{_free}(0, l), & 0 \le i \le n,\ j = 0\\
a_{j-i+n} \cdot \sum_{d=\lfloor i/n \rfloor}^{\lceil j/n \rceil} \text{all_}y\text{_free}(d, y_1), & 0 \le i \le n,\quad 1 \le j \le M-1\\
a_{j-i+n} \cdot \sum_{d=\lceil (i-n)/n \rceil}^{\lceil j/n \rceil} \text{all_}y\text{_free}(d, y_2), & n+1 \le i \le M,\quad i-n \le j \le M-1\\
\sum_{l=B-i+n}^{nN} a_l \cdot \sum_{d=\lfloor i/n \rfloor}^{\lceil j/n \rceil} \text{all_}y\text{_free}(d, y_3), & 0 \le i \le M,\quad j = M\\
0, & \text{otherwise}
\end{cases} \qquad (6)$$

where the values for y_1, y_2 and y_3 are given by

y_1

if $d = 0$, then $y_1 = n - i$

else if $d = \left\lceil \frac{j}{n} \right\rceil$, then $y_1 = j - (d-1)n$

else $y_1 = n$

y_2

if $\left\lceil \frac{i-n}{n} \right\rceil = \left\lceil \frac{j}{n} \right\rceil$, then $y_2 = l$

else if $d = \left\lceil \frac{i-n}{n} \right\rceil$, then $y_2 = 2n - i$

else if $d = \left\lceil \frac{j}{n} \right\rceil$, then $y_2 = j - (d-1)n$

else $y_2 = n$

y_3

if $d = 0$, then $y_3 = n - i$

else if $d = \left\lfloor \frac{i}{n} \right\rfloor$, then $y_3 = 2n - i$

else if $d = \left\lceil \frac{j}{n} \right\rceil$, then $y_3 = j - (d-1)n$

else $y_3 = n$.

In timeslot x, a delay of d timeslots associated with a third-stage wavelength converter is only available if no other packets are already scheduled to transmit during timeslot $x+d$ to the same converter. Consequently, the transition probability of having j cells in the queue at the end of timeslot x, given i cells at the end of timeslot $x-1$, is only possible if there is no exit time contention for any of the new arriving cells destined for the tagged output.

To illustrate the formulation of t_{ij}, consider, as an example, t_{12}, where $i = 1$, $j = 2$, and $n = N = 4$, i.e., the transition probability of having two packets in the queue at the end of

timeslot x given one packet at the end of timeslot $x-1$. From (6)—the equation for y_1

$$t_{ij} = a_{j-i+n} \cdot \sum_{d=\lfloor i/n \rfloor}^{\lceil j/n \rceil} \text{all\_}y\text{\_free}(d, y_1)$$

$$t_{12} = a_5 \cdot \sum_{d=0}^{1} \text{all\_}y\text{\_free}(d, y_1)$$

fulfilling condition for y_1, i.e.,

$$\text{when } d=0,\ y_1 = n - i = 4 - 1 = 3 \text{ and}$$
$$\text{when } d=1 \left(\text{i.e.} = \left\lceil \frac{j}{4} \right\rceil\right),$$
$$y_1 = j - (d-1)n = 2 - (1-1)n = 2$$

therefore

$$t_{12} = a_5 \cdot \sum_{d=0}^{1} \text{all\_}y\text{\_free}(d, y_1)$$
$$= a_5(\text{all\_}y\text{\_free}(0, 3) + \text{all\_}y\text{\_free}(1, 2))$$

where $\text{all\_}y\text{\_free}(0, 3)$ and $\text{all\_}y\text{\_free}(1, 2)$ can be obtained from (5). The probability of having two packets in the queue at the end of timeslot x if one packet exists at the end of timeslot $x-1$ is

1) the probability of having five incoming packets (i.e., $j - i + n$) destined to the tagged output;
2) no exit time blocking from packets scheduled in previous timeslots, which are routed out to zero-timeslot delays and one-timeslot delays.

Of the five incoming packets, three of them will be routed to zero-timeslot delays and another two to one-timeslot delays. Therefore, this transition is only possible if there is no exit time contention blocking for zero-timeslot delay for three of the incoming packets [i.e., $\text{all\_}y\text{\_free}(0, 3)$] and one-timeslot delay for another two [i.e., $\text{all\_}y\text{\_free}(1, 2)$], illustrated in Fig. 9.

Using the above state transition probability, the probability of having i cells in the queue at end of time slot m, q_i^x is given by [23]

$$\left[q_0^{x-1} \cdots\cdots q_M^{x-1}\right][t_{ij}] = [q_0^x \cdots\cdots q_M^x]. \tag{7}$$

Eliminating the time dependency, i.e., $q_i^{m-1} \Rightarrow q_i$, $q_i^m \Rightarrow q_i$, (7) gives $M+1$ linear equations, which will yield a trivial solution. These $M+1$ equations are linearly dependent and are redundant. Therefore, to obtain a nontrivial solution for qi, one of the $M+1$ equations can be replaced by $\sum_{i=0}^{M} q_i = 1$.

D. Packet Loss Probability

The cell success probability (CSR) is equal to $1-$CLR, where CLR is the cell loss probability. The cell success probability is the number of successfully transmitted cells divided by the mean number of cells that enter the queue in each timeslot. Assuming this, the number of successfully transmitted cells is

$$n - \lambda_{\text{unused}} \tag{8}$$

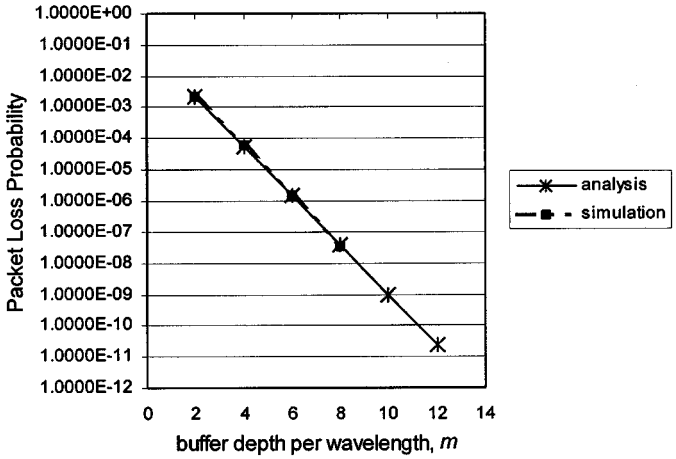

Fig. 10. Packet loss performance of the switch using AWGs and space switch under uniform traffic of 0.8 (analytical and simulation results) for $N = 16$, $n = 4$.

where λ_{unused} is the mean number of unused wavelengths, which is given by

$$\lambda_{\text{unused}} = \sum_{i=0}^{n} \sum_{j=0}^{n-i} a_j q_i.(n - (i+j)).$$

The mean number of cells arriving at the queue in each timeslot is given by

$$n\rho. \tag{9}$$

Combining (8) and (9), the cell success probability CSR is then

$$\text{CSR} = \frac{n - \lambda_{\text{unused}}}{n\rho}.$$

Finally, the cell loss probability CLR is given by

$$\text{CLR} = 1 - \text{CSR} = 1 - \frac{n - \lambda_{\text{unused}}}{n\rho}$$

and the mean delay DEL is

$$\text{DEL} = \frac{\sum_{d=1}^{B} q_d \cdot \left(\left\lfloor \frac{d}{n} \right\rfloor + 1\right)}{(n - \lambda_{\text{unused}})\rho}.$$

V. Verification and Results

The performance of the switch was obtained using the above analytical framework for uniform Bernoulli traffic. Packet loss performance was also evaluated for bursty traffic (exponentially distributed packet inter arrival time) using the Monte Carlo approach. Furthermore, it is shown that simulation justifies the analysis.

Figs. 10 and 11 show both the analytical and simulation results for a 16×16-switch packet loss and delay with four wavelengths per input at a uniform traffic load of 0.8 per wavelength channel, respectively. The packet loss probability is less than 10^{-9} with a buffer depth per wavelength of 10 or more,

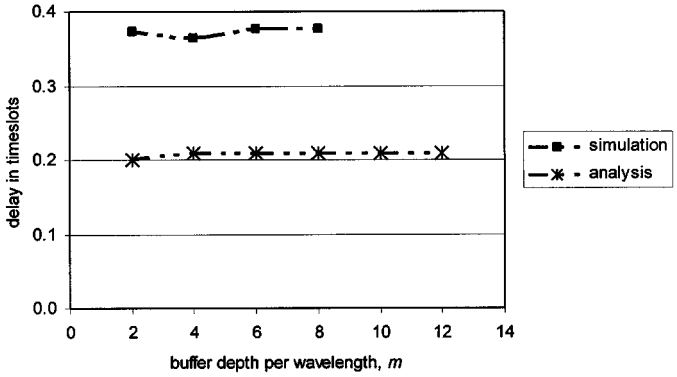

Fig. 11. Delay performance under uniform traffic of 0.8 (analytical and simulation results) for $N = 16, n = 4$.

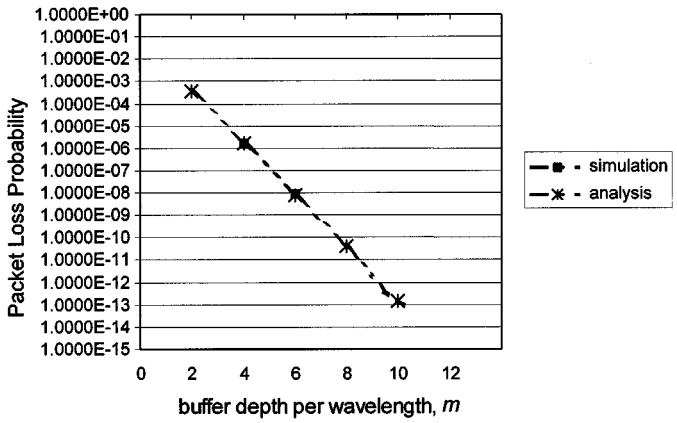

Fig. 12. Packet loss performance under uniform traffic of 0.8 (analytical and simulation results) for $N = 32, n = 6$.

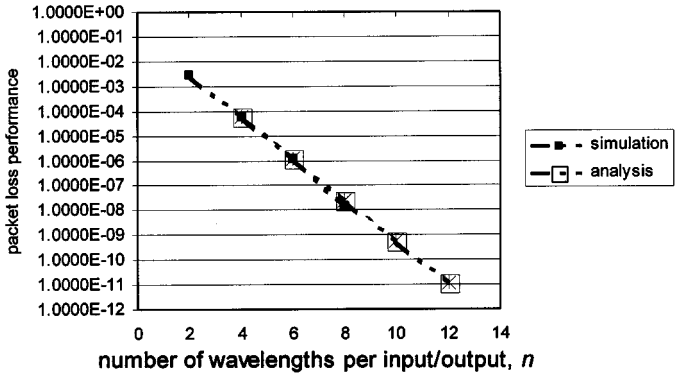

Fig. 13. Packet loss performance under uniform traffic of 0.8 (analytical and simulation results) for $N = 16, m = 4$.

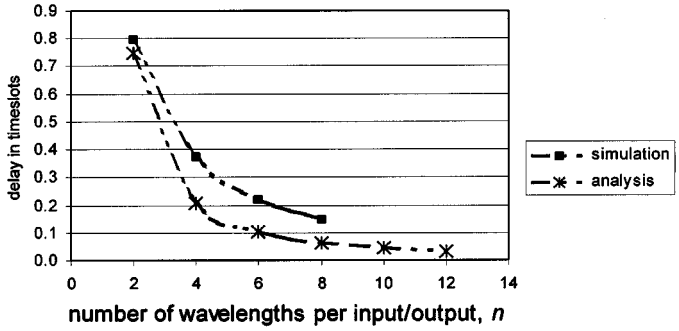

Fig. 14. Delay performance under uniform traffic of 0.8 (analytical and simulation results) for $N = 16, m = 4$.

thus requiring 10 uniform[1] delay lines (or more) in each set of delay lines. The mean delay is less than 0.4 timeslots with the same buffer depth per wavelength. The analytical results for the packet loss probability match well with the simulation. There is a discrepancy between delay performance in the analysis and simulation, since the analysis does not exactly model the delay dependency between the blocked packets in the buffer. The blocked packets affect the scheduled delays of the subsequent packets destined to the same output port due to the FIFO scheduling algorithm. Therefore, the analysis underestimates the delay performance.

For 32 inputs–outputs with six wavelengths per input or output, the packet loss probability becomes less than 10^{-13} for a buffer depth per wavelength of 10 or more (Fig. 12).

As expected, packet loss and delay performance improve with increasing number of wavelength channels per input (Figs. 13 and 14). For a 16×16 switch with a buffer depth per wavelength of four at a uniform traffic load of 0.8 per wavelength, the loss probability improves to less than 10^{-9} with more than 10 wavelengths per input, compared to 10^{-4} with four wavelengths per input (Fig. 13). In addition, the delay performance decreases with increasing number of wavelengths per input (Fig. 14).

Fig. 15 shows the packet loss performance improvement with increasing number of wavelengths per input for a 32×32 switch with a buffer depth per wavelength of four and at a uniform traffic load of 0.8 per wavelength. The packet loss probability is 10^{-6} and 10^{-9} with six and 10 wavelengths per input, respectively.

In addition, the switch packet loss performance was also evaluated by simulation under bursty traffic with a mean burst length of four. As expected, the performance degrades markedly from that obtained under uniform traffic (Fig. 16). For a switch size of 16 inputs or outputs with four wavelengths per input and a traffic load of 0.8 per wavelength, the packet loss probability increases to 10^{-2}, compared to 10^{-6} under uniform traffic for a buffer depth of six per wavelength.

Under bursty traffic, a 16×16 switch with four wavelengths per input needs 200 buffer locations per wavelength to achieve a packet loss probability of less than 10^{-6}. The packet loss probability improves to 10^{-6}, with 16 wavelengths per input and a buffer depth per wavelength of 40. In [15], it is shown that the packet loss performance improves significantly under bursty traffic if the difference in successive delay line lengths is increased. Its packet loss performance approaches that under uniform traffic with a larger D (≈ 10). The larger D is, the larger the switch latency is but the switch size remains the same.

VI. Conclusion

In this paper, architectures for optical packet switches have been proposed that aim to circumvent the large optical splitting loss inherent in many designs by using AWG devices. Two configurations have also been proposed: feed-forward delay lines and feedback delay lines, both easily modified to handle WDM inputs–outputs. The feedback architecture is expected to have

[1]The difference in the length of successive delay lines is one timeslot.

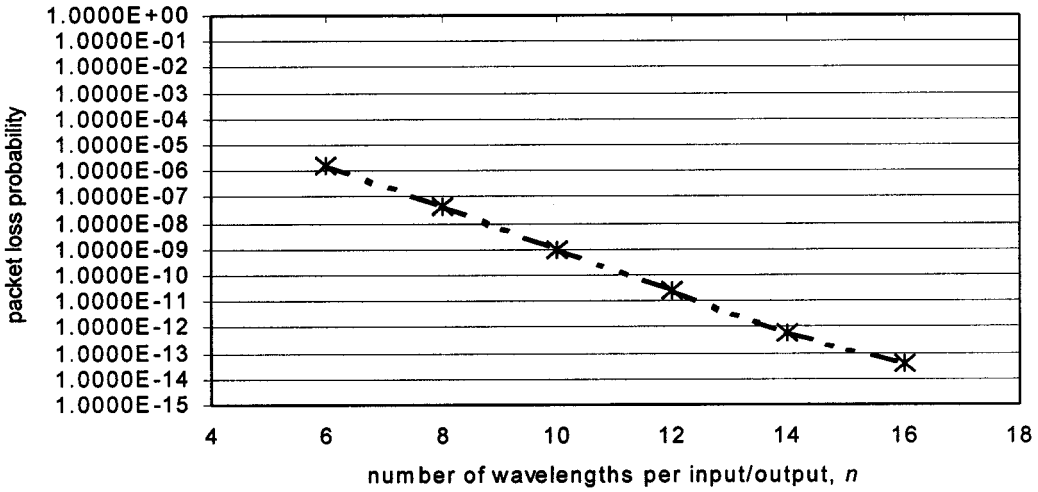

Fig. 15. Packet loss performance under uniform traffic of 0.8 (analytical results) for $N = 32$, $m = 4$.

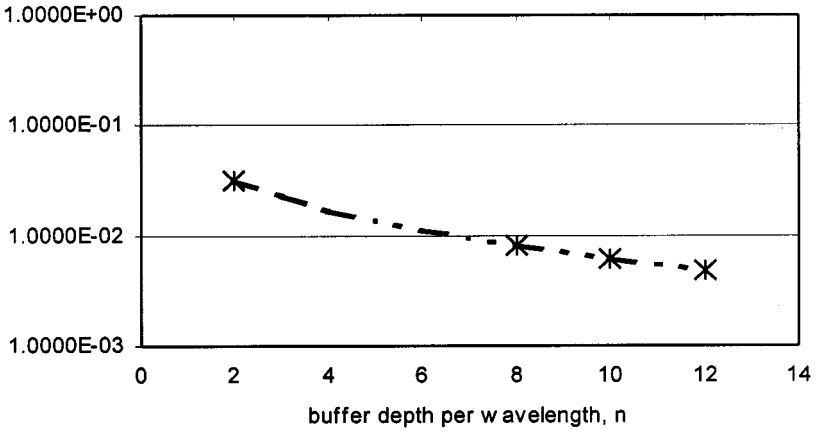

Fig. 16. Packet loss performance under bursty traffic with mean burst length of four and load 0.8 (simulation results) for $N = 16$, $n = 4$.

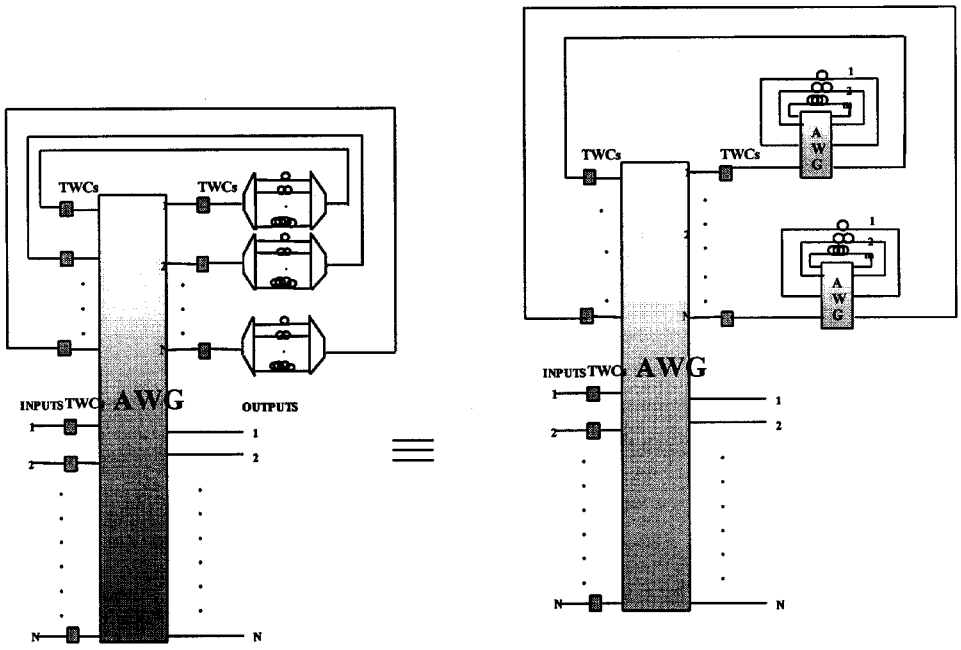

Fig. 17. The simplified design with N AWGs with feedback delay lines in the node feedback loop.

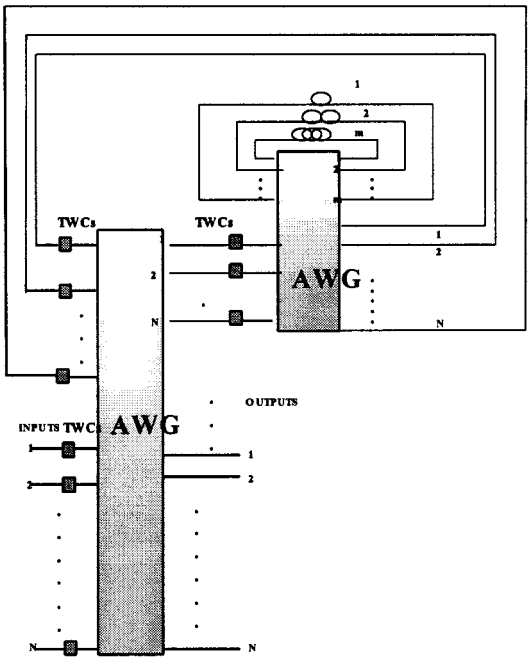

Fig. 18. The further simplified node design with only one AWG in the feedback loop.

poorer optical performance than the feed-forward configuration because a larger AWG is used, thus increasing the number of crosstalk terms. However, the feedback configuration enables the implementation of priority routing, where the high-priority packets can preempt low-priority ones. Selected inputs of the AWG may be left unused in order to reduce or even eliminate homowavelength crosstalk [26].

In terms of the proposed node packet loss performance, for 32 inputs–outputs with six wavelengths per input or output, the packet loss probability is less than 10^{-13} for a buffer depth per wavelength of 10 or more with a uniform Bernoulli traffic load of 0.8 per wavelength. The packet loss and delay performances improve as the number of wavelength channels per input is increased.

The N units (each consisting of a demultiplexer, delay lines, and a multiplexer) can be replaced by an $(m+1) \times (m+1)$ AWG with feedback delay lines (Fig. 17). The proposed node design can be further simplified by amalgamating the functions of all N AWGs in the feedback loop into only one AWG of size $m+N$ (Fig. 18), referred to as the "second AWG." If two or more packets want to use the same delay in the feedback loop of the second AWG, they have to be routed to different inputs of the second AWG in order to access the same delay using different wavelengths.

Experimental verification of the functionality of the switch has also been undertaken successfully within the WASPNET project [27].

APPENDIX

Here, which_delay identifies the delay lines (in the set of delay lines identified by the parameter which_set) corresponding to the delay that the packet destined for switch output i should undergo, solving output port contention and keeping the packet sequences within an optical path. After determining the delay in order to preserve the packet sequences and avoid output port contention, parameter which_set indicates the set of delay lines exhibiting no exit time contention for the assigned delay value of which_delay. The delay that the packet should experience is dependent on the delay of the last packet destined for the same output, to preserve FIFO. Therefore, when a packet arrives at timeslot j, the control will schedule the packet according to the value of which_delay (which_delay $= x$ in the following pseudocode) of the destined output; the delay that the new packet should be stored is then which_delay. The control has to find the set of delay lines that has no exit time contention for the arriving packet by examining the first set of delay lines (i.e., which_set $= 1$) until a set of delay lines is available that matches the delay value of which_delay. If no set of delay lines (which_set $= N$) is available, the packet should be stored in longer delay lines (which_delay $= x+1$), and if all sets of delay lines for all delay values of which_delay are not available, the packet is then lost.

```
Scheduling Stage
    which_delay = x      ** let x be the delay line that has the same delay as the last packet destined for the same
                         output/optical path at the end of timeslot m − 1, to preserve FIFO operation; i.e.,
                         0 ≤ x ≤ max_delay where max_delay is the maximum number of delay lines in each set of delay
                         lines. If this is the first packet being scheduled on this timeslot for a particular output, x will be
                         equal to 0.
    if a packet arrives at timeslot m destined for output i
    {
      which_set = 1      **which_set identifies a set of fiber delay lines, hence 1 ≤ which_set ≤ max_set

      while (TRUE)             **loop until exit via return statement
                               **go through each set of fiber delay lines (i.e., the first-stage AWG's output)
      {
```

```
            if no exit time contention for the value of the assigned which_delay
            {
               route the packet to this delay line by:
                  1. converting its wavelength to be switched to this set of fiber delay lines via the first AWG
                  2. converting its wavelength again so it is routed to this delay line using the corresponding second stage
                     of tunable wavelength converter.

               return packet routed   ** terminate the while loop because the scheduling is completed
            }
            else                      **if there is exit time contention
            {

               which_set = which_set + 1        **go to the same delay line in the next set of fiber delay lines
              if which_set > max_set            **all sets of delay lines have exit time contention
              {
                  which_delay = which_delay + 1  **go to a longer delay line

                  if which_delay > max_delay
                  return packet lost             **buffer overflow and terminate the while loop
                  else
                     which_set = 1               **no buffer overflow and go through each set of delay lines again
                                                  for the new which_delay values
              }
            }
      }           **end while loop for which_set
      }
   else                    **no packet arrives for output i
      x = max(x - 1, 0)    **decrease the delay counter for output i
```

Switching Stage

```
   for each input of the space switch
      if a packet arrives from the delay lines
         route the packet to the corresponding output by:
          • converting its wavelength to the transmission wavelength and then routing through the space switch
      endif
      go to next input
   endfor
```

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